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Title:

A LOW VOLTAGE CURRENT REFERENCE

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A LOW VOLTAGE CURRENT REFERENCE

FIELD OF THE INVENTION

[0001] The present invention relates in general to reference current generation circuits for semiconductor devices, and more particularly to a reference current generation circuit for outputting a nearly constant current across a range of temperatures and input voltages.

BACKGROUND OF THE INVENTION

[0002] Technological improvements in semiconductor processing have led to a substantial increase in the number of transistors fabricated on a single integrated circuit. Along with an increase in the number of transistors also comes an increase in the amount of power dissipated by the integrated circuit. In an effort to reduce power dissipation and consumption, engineers have reduced the voltage level of the power supplies in such integrated circuits, from the traditional 5 volts to about 3.3 volts. This trend is expected to continue. Some current integrated circuits, for example microprocessors, operate at least a portion of their circuitry voltages below 3.3 volts. It is expected that more and more integrated circuits will be operated at power supply voltages below 3.3 volts.

[0003] Many integrated circuits are increasingly using mixed signal circuits (e.g. digital and analog) to perform various functions, such as voltage or current controlled

oscillators. In addition, other circuits such as D/A (digital-to-analog) converters and multipliers may be employed in integrated circuits. Non-volatile memories, such as flash memories, include a digital portion for reading and accessing data and an analog portion for erasing. These designs generally require a reference current which is relatively stable across a range of operating temperatures and power supply voltages. With the increasing use of low-level power supply voltages, it is even more difficult to provide a needed stable current reference.

[0004] Accordingly, there is a need for a current reference which provides stable current over a range of operating temperatures and power supply voltages for use in integrated circuits.

SUMMARY OF THE INVENTION

[0005] The present invention provides for a current reference which provides a stable output current over a range of operating temperatures and power supply voltages for use in an integrated circuit. The current reference is comprised of a first current generation subcircuit having a negative thermal coefficient, a second current generation subcircuit having a positive thermal coefficient, a summing circuit controlled by the first and second current generation subcircuits, and an output circuit.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is a schematic diagram of a current reference in accordance with the principles of the present invention;

[0007] FIG. 2 is a graph illustrating how the current I2 inside the first current generation subcircuit varies across a range of temperatures and input voltages;

[0008] FIG. 3 is a graph illustrating how the current I4 inside the second current generation subcircuit varies across a range of temperature and input voltages;

[0009] FIG. 4 is a graph illustrating how the current I5 inside the output circuit varies across a range of temperature and input voltages;

[0010] FIG. 5 is an illustration memory device incorporating the current reference illustrated in FIG. 1; and

[0011] FIG. 6 is an illustration of a processor based system incorporating a memory device of FIG. 5.

DETAILED DESCRIPTION

[0012] Now referring to the drawings, where like reference numerals designate like elements, FIG. 1 is a schematic diagram of a current reference 100 in accordance with the principles of the present invention. The current reference includes a first current generation subcircuit 110, a second current generation subcircuit 130, a summing circuit 150 controlled by the first and second current generation subcircuits 110,130, and an output circuit 170. Input power (e.g., Vcc) is supplied from an input power terminal 101. The temperature compensation for current reference 100 is obtained by summing the current control signals from the first and second subcircuits 110, 130. The first current generation subcircuit 110 provides a control signal which allows the summing circuit 150 to generate a current component (e.g., current I5 in MOSFET 151) with a negative thermal coefficient, while the second current generation subcircuit 130 provides a control signal which allows the summing circuit 150 to generate a current component (for example, I6 in MOSFET 152) with a positive thermal coefficient.

[0013] The first current generation subcircuit 110 is a ΔVt circuit (where ΔVt represents the difference in threshold voltage of two FET transistors) and comprises two PMOS transistors 111-112 arranged in a current mirror configuration to deliver indentical currents I1, I2 to two NMOS transistors 115-116 having different threshold voltages. The two PMOS transistors 111-112 have their gates coupled together at node 113, and the

drain of PMOS transistor 112 is coupled to the gates of PMOS transistors 111-112 via a coupling between node 113 and node 114. The current mirror formed by this arrangement ensures that current I1, the current flowing from the drain of PMOS transistor 111 to NMOS transistor 115, is identical to current I2, the current flowing from the drain of PMOS transistor 112 and NMOS transistor 116.

[0014] The gates of the NMOS transistors 115-116 are coupled together at node 117. Node 117 is also coupled to the drain of PMOS transistor 111 and the drain of NMOS transistor 115 at node 118. The source of NMOS transistor 115 is coupled to ground potential at node 120, while the source of NMOS transistor 116 is coupled to ground at node 121 through register 119.

[0015] As described above, the two NMOS transistors are to have different threshold voltages. In one embodiment, NMOS transistor 116 has a higher threshold voltage than NMOS transistor 115. The difference in threshold voltage between NMOS transistors 115-116 can be obtained using any suitable fabrication technique. For example, in one embodiment, thickness of the oxide layer of the NMOS transistor 115 is approximately twice the thickness in the oxide layer of NMOS transistor 116.

[0016] Input power is supplied to the first current generation subcircuit 110 via the input power terminal 101. In the first current generation subcircuit 110, with current I1 equal to current I2, the current I2 is governed by the following equation:

[0017] $I2 = [\ Vt(115, T) - Vt(116,T)\ ] / R(119,T)$ (1)

[0018] where:

[0019] Vt(115, T) is the threshold voltage of transistor 115, which is temperature dependent;

[0020] Vt(116, T) is the threshold voltage of transistor 116, which is temperature dependent; and

[0021] R(119,T) is the resistance of resistor 119, which is temperature dependent.

[0022] While the threshold voltages of the transistors, Vt(115, T) and Vt(116, T), vary with a negative thermal coefficient, the resistance of resistor 119 also varies according to temperature. Resistor 119 (and also resister 139 of the second current generation subcircuit 130) may be a conventional type of resistor with a positive thermal coefficient. That is, the resistance of the resistor increases as temperature increases and the resistance decreases as temperature decreases. The first current generation subcircuit 110 is designed so that the current I2 has a negative thermal coefficient, i.e., the current I2 tends to decrease as the temperature increases. As illustrated in FIG. 2, in one embodiment, the current I2 decreases linearly from approximately 8 micro ampere to 1.8 micro ampere as the temperature increases from -40 degrees to +90 degrees Celsius, respectively.

[0023] Thus, as temperatures increase, the current I2 decreases, causing the voltage at node 114 to increase. Likewise, as temperatures decrease, the current I2 increases, causing the voltage at node 114 to decrease. Since node 114 is coupled to the gate of PMOS transistor 151, the voltage applied to a portion of the summing circuit 150 is controlled in an inverse proportional manner by the temperature of the first current generation subcircuit 110.

[0024] The second current generation subcircuit 130 provides a control signal to the summing circuit 150 to generate a current component (e.g., current I6 in MOSFET 152) with a positive thermal coefficient (i.e., the inverse of the control signal generated by the first current generation circuit). The second current generation subcircuit 130 provides a control signal which allows the summing circuit 150 to generate a current component (e.g., current I6 in MOSFET 152) with a positive thermal coefficient (i.e., the inverse of the control signal generated by the first current generation subcircuit 110). The second generation subcircuit 130 comprises two PMOS transistors 131-132 arranged in a current mirror configuration to deliver identical currents I3 and I4 to two bipolar transistors 135-136. The two PMOS transistors 131-132 have their gates coupled together at node 133, and the drain of PMOS transistor 132 is coupled to the gates of PMOS transistors 131-132 via a coupling between nodes 133 and node 134. The current mirror formed by this arrangement ensures that current I3, the current flowing from the drain of PMOS

transistor 131 to bipolar transistor 135, is identical to current I4, the current flowing from the drain of PMOS transistor 132 and bipolar transistor 136.

[0025] The gates of bipolar transistors 135-136 are coupled together at node 137. Node 137 is also coupled to the drain of PMOS transistor 131 and the base of bipolar transistor 135 at node 118. The emitter of the bipolar transistor 135 is coupled to ground potential at node 140, while the emitter of the bipolar transistor 116 is coupled to ground at node 141 through resister 139.

[0026] Input power is supplied at the source of PMOS transistors 131-132 via the input power terminal 101. In the second current generation subcircuit 130, the current I4 is governed by the following equation:

[0027] $$I4 = [Vbe(135) - Vbe(136)] / R(139,T) \qquad (2)$$

[0028] where:

[0029] Vbe(135) is the base-to-emitter voltage of bipolar transistor 135;

[0030] Vbe(136) is the base-to-emitter voltage of bipolar transistor 136; and

[0031] R(139,T) is the resistance of resistor 139.

[0032] If the current flowing through the bipolar transistors 135-136 are identical, it can be demonstrated that:

[0033] $$I4 = [(K * T / q) * \ln(A2/A1)] / R(139,T) \quad (3)$$

[0034] where:

[0035] K is Boltzman's constant;

[0036] q is the charge of an electron;

[0037] T is temperature (in degrees Kelvin);

[0038] A1 is the emitter area of transistor 135; and

[0039] A2 is the emitter area of transistor 136.

[0040] As can be seen from equation (3), the current I4 has a positive thermal coefficient, i.e., the current I4 increases as the temperature increases. In one embodiment, illustrated in FIG. 3, current I4 increases linearly from approximately 18.2 micro amps to 24.8 micro amps as the temperature increases from -40 degrees to +90 degrees Celsius, respectively. Thus, as temperature increases, the current I4 increases, causing the voltage at node 134 to decrease. Likewise, as temperature decreases, the current I4 decreases, causing the voltage at node 134 to increase. Since node 114 is coupled to the gate of PMOS transistor 151, the voltage applied to a portion of the summing circuit 150 is controlled in an inverse proportional manner by the temperature of the second current generation subcircuit 130.

[0041] The summing circuit 150 is comprised of a pair of PMOS transistors 151-152 which respectively control the amount of current delivered from the input power terminal to the node 153. More specifically, the current in the transistor 151 is controlled by the first current generation subcircuit 110 while the current of PMOS transistor 152 is controlled by the second current generation subcircuit 130. As noted above, the first and second current generation subcircuits 110, 130 are designed to react to temperature changes in opposite fashions. Thus any change in temperature will cause the current of one of the PMOS transistors 151, 152 to increase while the current in the other one of the PMOS transistors 151,152 decreases, thereby providing a temperature independent source of current available at node 153.

[0042] The output circuit is coupled to the output node 153 of the summing circuit and comprises an output terminal 172 where a reference voltage bias is provided (to bias gate terminal of external NMOS transistors). The output terminal is coupled to the gate of a NMOS transistor 171 via node 173, which is also coupled to the drain of the NMOS transistor 171 and the output node 153 of the summing circuit.

[0043] Thus, the current reference of the present invention is comprised of two current generation subcircuits 110, 130 which produce control voltages for adjusting the gains two transistors 151-152 in a summing circuit 150. Each current generation subcircuit comprises two PMOS transistors which form a current mirror. The current

flowing through the current mirrors of each subcircuit flows through a difference circuit formed of two additional transistors and one resistor, which is dependent upon temperature. However, in one subcircuit, the current flow has a negative thermal coefficient, while in the other subcircuit the current flow has a positive thermal coefficient. The design of the generation subcircuits and the summing circuit provides the output circuit with a power supply which is stable across a range of temperatures and input voltages.

[0044] FIG. 5 is a block diagram of a memory device 500 including the current reference 100 of FIG. 1. The memory device includes a power line 501 for supply power to the memory device 500, a control bus 501, an address bus 502, and a data bus 503. The power line 501 is coupled to the current reference 100, which outputs temperature compensated power to various components of the memory device. These component may include a control circuit 510, an I/O circuit 520, and a memory array 530.

[0045] FIG. 6 illustrates an exemplary processing system 900 which may utilize a memory device 500 having a current reference 100 of the present invention. The processing system 900 includes one or more processors 901 coupled to a local bus 904. A memory controller 902 and a primary bus bridge 903 are also coupled the local bus 904. The processing system 900 may include multiple memory controllers 902 and/or multiple

primary bus bridges 903. The memory controller 902 and the primary bus bridge 903 may be integrated as a single device 906.

[0046] The memory controller 902 is also coupled to one or more memory buses 907. Each memory bus accepts memory components 908 which include at least one memory device 500 of the present invention. The memory components 908 may be a memory card or a memory module. Examples of memory modules include single inline memory modules (SIMMs) and dual inline memory modules (DIMMs). The memory components 908 may include one or more additional devices 909. For example, in a SIMM or DIMM, the additional device 909 might be a configuration memory, such as a serial presence detect (SPD) memory. The memory controller 902 may also be coupled to a cache memory 905. The cache memory 905 may be the only cache memory in the processing system. Alternatively, other devices, for example, processors 901 may also include cache memories, which may form a cache hierarchy with cache memory 905. If the processing system 900 include peripherals or controllers which are bus masters or which support direct memory access (DMA), the memory controller 902 may implement a cache coherency protocol. If the memory controller 902 is coupled to a plurality of memory buses 907, each memory bus 907 may be operated in parallel, or different address ranges may be mapped to different memory buses 907.

[0047] The primary bus bridge 903 is coupled to at least one peripheral bus 910. Various devices, such as peripherals or additional bus bridges may be coupled to the peripheral bus 910. These devices may include a storage controller 911, an miscellaneous I/O device 914, a secondary bus bridge 915, a multimedia processor 918, and an legacy device interface 920. The primary bus bridge 903 may also coupled to one or more special purpose high speed ports 922. In a personal computer, for example, the special purpose port might be the Accelerated Graphics Port (AGP), used to couple a high performance video card to the processing system 900.

[0048] The storage controller 911 couples one or more storage devices 913, via a storage bus 912, to the peripheral bus 910. For example, the storage controller 911 may be a SCSI controller and storage devices 913 may be SCSI discs. The I/O device 914 may be any sort of peripheral. For example, the I/O device 914 may be an local area network interface, such as an Ethernet card. The secondary bus bridge may be used to interface additional devices via another bus to the processing system. For example, the secondary bus bridge may be an universal serial port (USB) controller used to couple USB devices 917 via to the processing system 900. The multimedia processor 918 may be a sound card, a video capture card, or any other type of media interface, which may also be coupled to one additional devices such as speakers 919. The legacy device interface 920 is used to

couple legacy devices, for example, older styled keyboards and mice, to the processing system 900.

[0049] The processing system 900 illustrated in FIG. 6 is only an exemplary processing system with which the invention may be used. While FIG. 6 illustrates a processing architecture especially suitable for a general purpose computer, such as a personal computer or a workstation, it should be recognized that well known modifications can be made to configure the processing system 900 to become more suitable for use in a variety of applications. For example, many electronic devices which require processing may be implemented using a simpler architecture which relies on a CPU 901 coupled to memory components 908 and/or memory devices 100. These electronic devices may include, but are not limited to audio/video processors and recorders, gaming consoles, digital television sets, wired or wireless telephones, navigation devices (including system based on the global positioning system (GPS) and/or inertial navigation), and digital cameras and/or recorders. The modifications may include, for example, elimination of unnecessary components, addition of specialized devices or circuits, and/or integration of a plurality of devices.

[0050] The above description and accompanying drawings are only illustrative of exemplary embodiments, which can achieve the features and advantages of the present invention. It is not intended that the invention be limited to the embodiments shown and

described in detail herein. The invention can be modified to incorporate any number of variations, alterations, substitutions or equivalent arrangements not heretofore described, but which are commensurate with the spirit and scope of the invention. The invention is only limited by the scope of the following claims.